

DESCRIPTION

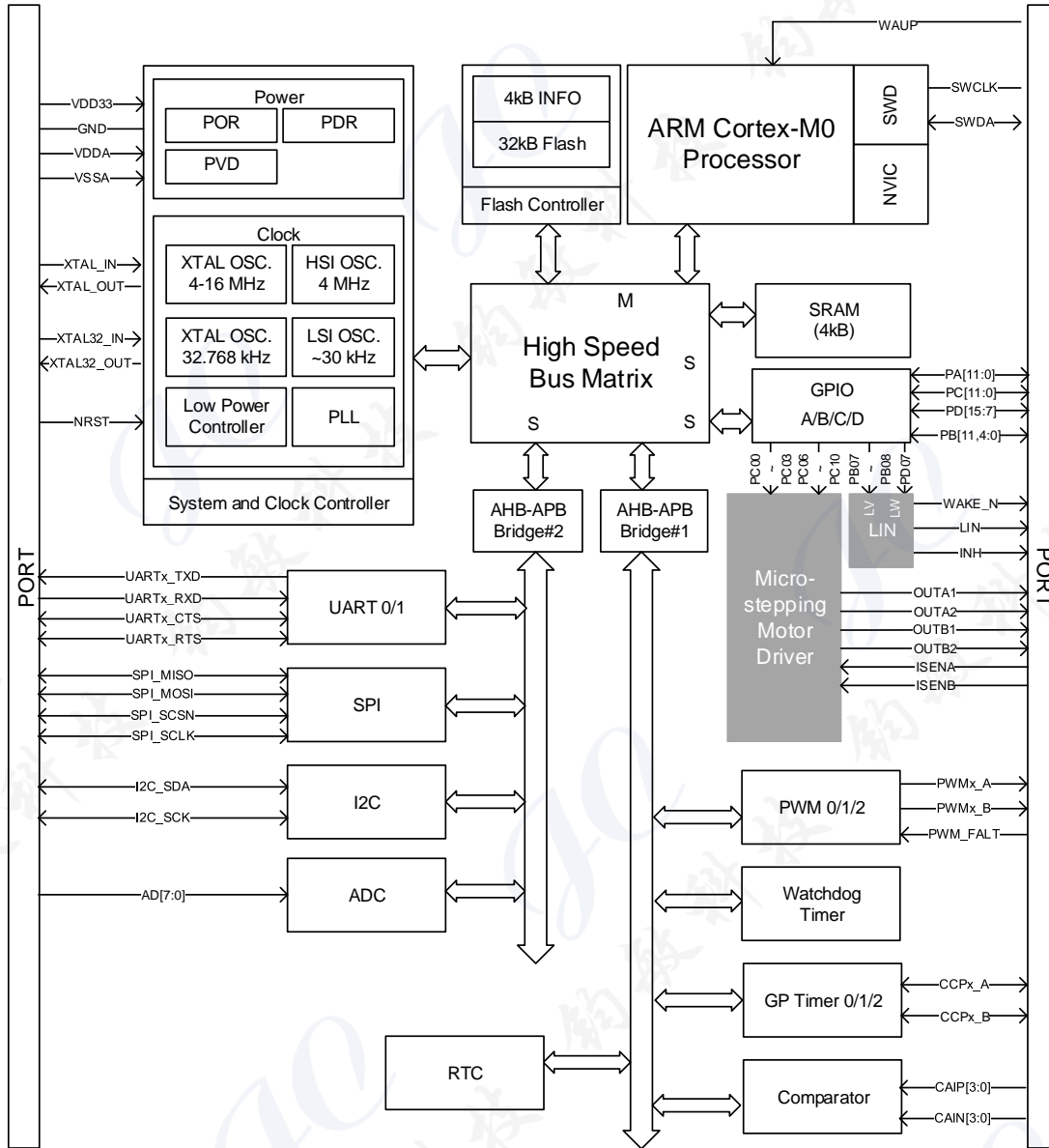
The PT32C637 is a SiP (System in Package) with ARM Cortex M0 MCU, a motor driver and a physical layer transceiver of Local Interconnect Network (LIN). The PT32C637 microcontroller is a series of low-power microcontroller incorporating a high-performance ARM Cortex™-M0 32-bit RISC core. It operates at a maximum 48MHz frequency and features up to 32Kbytes of Flash and up to 4Kbytes of SRAM. The Micro Stepping Motor Driver is designed for printers, scanners, and home and office automated equipment. The dual H-bridge drivers are consisting by all of N-channel MOSFETs, and designed to drive a 4-wires bipolar stepper motor. The output driving current of this stepping motor driver allows up to 1.6 Amps (mounted on dual layer PCB with proper heatsinking, VM=24V, TA=25°C).

The LIN is compliant with LIN 2.0/LIN 2.1/LIN 2.2/LIN 2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards. It is typically used for low speed in-vehicle networks using baud rates from 1 kBd to 20 kBd.

FEATURES

- ARM Cortex M0 Processor
- Performance up to 48 MHz
- Flash Memory 32K-Byte
- System SRAM 4K-Byte
- PWM Mode control logic
- Micro Stepping Motor Driver
 - 7.4-V to 45-V Supply Voltage Range
 - 1.6-A Maximum Driving Current at VM=24V (with additional heatsink)
 - Dual H-Bridge Driver for bipolar stepper motor with such features:
 - PWM chopping constant current regulation
 - Built-In micro stepping sequencer
 - Multiple micro steps, Full, 1/2, 1/4, 1/8, 1/16 and up to 1/32 steps
 - STEP and DIR logic inputs can control stepping motor revs and direction.
 - Winding current decay modes:
 - Mixed Decay
 - Slow Decay
 - Fast Decay
 - Built In a 3.3V reference voltage output
 - Low-power sleep mode
 - Protection Features
 - Over Current Protection (OCP)
 - Thermal Shutdown (TSD)
 - VM Under Voltage Lock Out (UVLO)
 - Fault Indication Pin (FAULTN)
- LIN
 - LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
 - Thermally protected
 - Transmit data (TXD) dominant time-out function
 - Bus terminal current limit protected
 - Very low current consumption in Sleep mode
 - Support local and remote wake-up
 - Enable an external high voltage regulator by INH
 - Baud rates up to 20 kBd
 - Very low ElectroMagnetic Emission (EME)
 - High ElectroMagnetic Immunity (EMI)

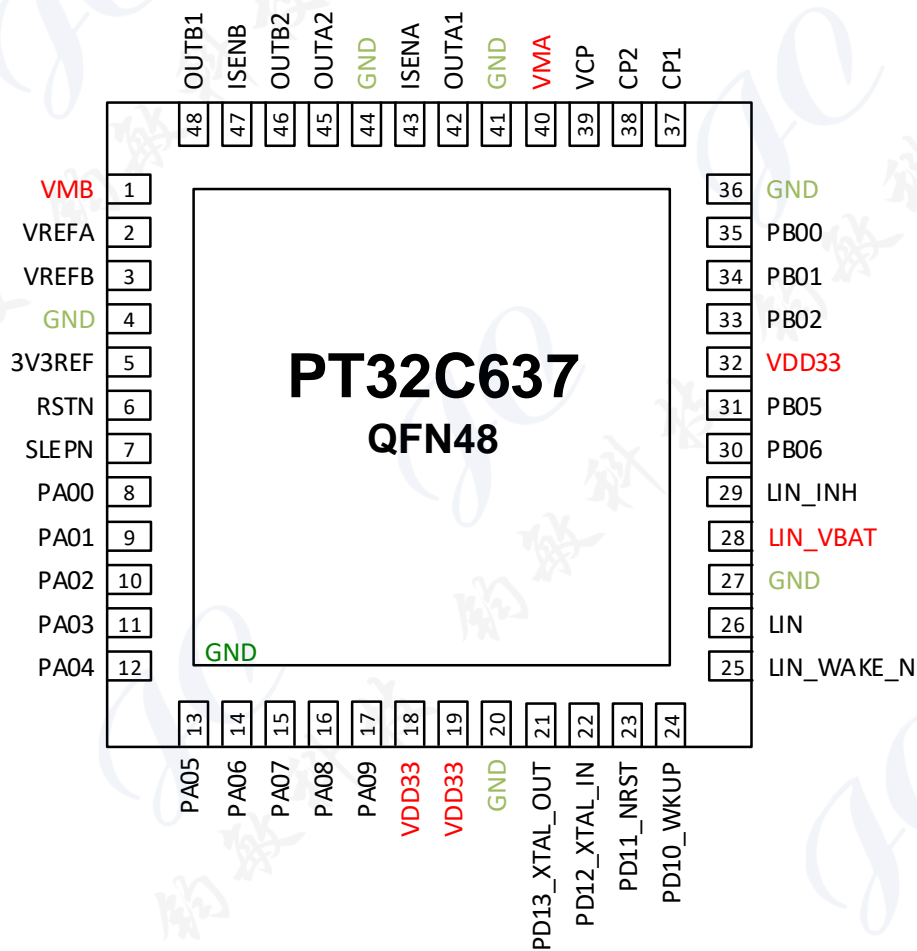
BLOCK DIAGRAM



1. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT32C637	QFN 48	PT32C637-

2. PIN CONFIGURATION



3. PIN DESCRIPTION

Each GPIO line can be assigned to one of the peripheral functions. The following table lists out the pin name of all packages and its respective available alternate function.

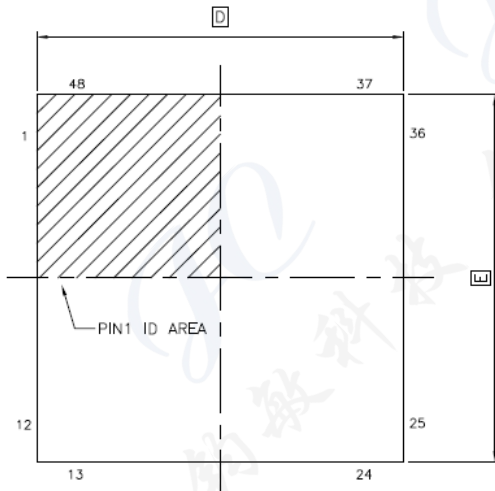
Pin Name	Pin Type	Description	Pin No.
VMB	Supply	Motor driver: H-Bridge B power supply	1
VREFA	I	Motor driver: H-Bridge A current set reference input	2
VREFB	I	Motor driver: H-Bridge B current set reference input	3
GND	Ground	Motor driver ground	4
3V3REF	O	Motor driver:3.3V reference voltage output	5
RSTN	I	Motor driver: Reset input (L=Initialize all of internal logic registers and disables H-bridge outputs)	6
SLEPN	I	Motor driver: Sleep mode input (H=device enable, L=low-power sleep mode)	7
PA00	I/O	General Purpose Digital I/O Pin	8
PA01	I/O	General Purpose Digital I/O Pin	9
PA02	I/O	General Purpose Digital I/O Pin	10
PA03	I/O	General Purpose Digital I/O Pin	11
PA04	I/O	General Purpose Digital I/O Pin	12
PA05	I/O	General Purpose Digital I/O Pin	13
PA06	I/O	General Purpose Digital I/O Pin	14
PA07	I/O	General Purpose Digital I/O Pin	15
PA08	I/O	General Purpose Digital I/O Pin	16
PA09	I/O	General Purpose Digital I/O Pin	17
VDD33	Supply	3.3V Voltage Supple	18
VDD33	Supply	3.3V Voltage Supple	19
GND	Ground	Ground	20
PD13_XTAL_OUT	I/O	General Purpose Digital I/O Pin	21
PD12_XTAL_IN	I/O	General Purpose Digital I/O Pin	22
PD11_NRST	I/O	General Purpose Digital I/O Pin	23
PD10_WKUP	I/O	General Purpose Digital I/O Pin	24
LIN_WAKE_N	I	LIN: local wake-up input (active LOW); negative edge triggered.	25
LIN	I/O	LIN bus line input/output.	26
GND	Ground	Ground	27
LIN_VBAT	Supply	Battery supply voltage.	28
LIN_INH	O	Battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event.	29
PB06	I/O	General Purpose Digital I/O Pin	30
PB05	I/O	General Purpose Digital I/O Pin	31
VDD33	Supply	3.3V Voltage Supple	32
PB02	I/O	General Purpose Digital I/O Pin	33
PB01	I/O	General Purpose Digital I/O Pin	34
PB00	I/O	General Purpose Digital I/O Pin	35
GND	Ground	Ground	36
CP1	I	Motor driver: External flying capacitor for charge pump, Connect a 0.01 μ F/50V low-ESR ceramic capacitor between CP1 and CP2.	37
CP2	I		38
VCP	O	Motor driver: High-side gate drive supply voltage (Connect a 0.1 μ F/50V ceramic capacitor and a 1M Ω resistor to VM.)	39
VMA	Supply	Motor driver: H-Bridge A power supply	40
GND	Ground	Ground	41
OUTA1	O	Motor driver: H-Bridge A output 1	42
ISENA	I	Motor driver: H-Bridge A current sense / GND	43
GND	Ground	Ground	44

Pin Name	Pin Type	Description	Pin No.
OUTA2	O	Motor driver: H-Bridge A output 2	45
OUTB2	O	Motor driver: H-Bridge B output 2	46
ISENB	I	Motor driver: H-Bridge B current sense / GND	47
OUTB1	O	Motor driver: H-Bridge B output 1	48

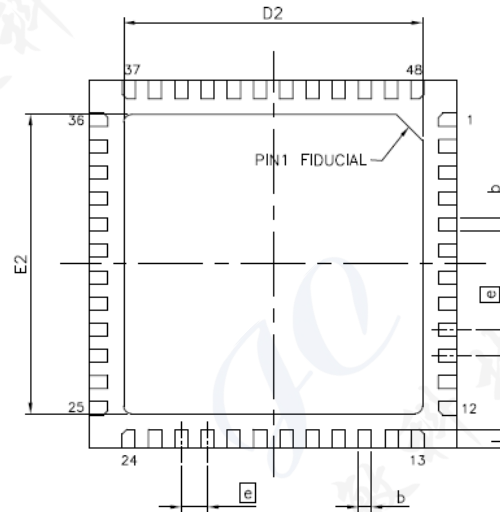
4. PACKAGE INFORMATION

48-PIN, QFN, 7 X 7

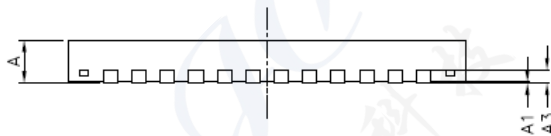
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.60	5.70	5.80
E2	5.60	5.70	5.80
e	0.50 BSC		
L	0.25	0.35	0.45

IMPORTANT NOTICE

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Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian, Dist., New Taipei City 23145, Taiwan
Tel : 886-2-66296288
Fax: 886-2-29174598
<http://www.princeton.com.tw>